

FIG. 1

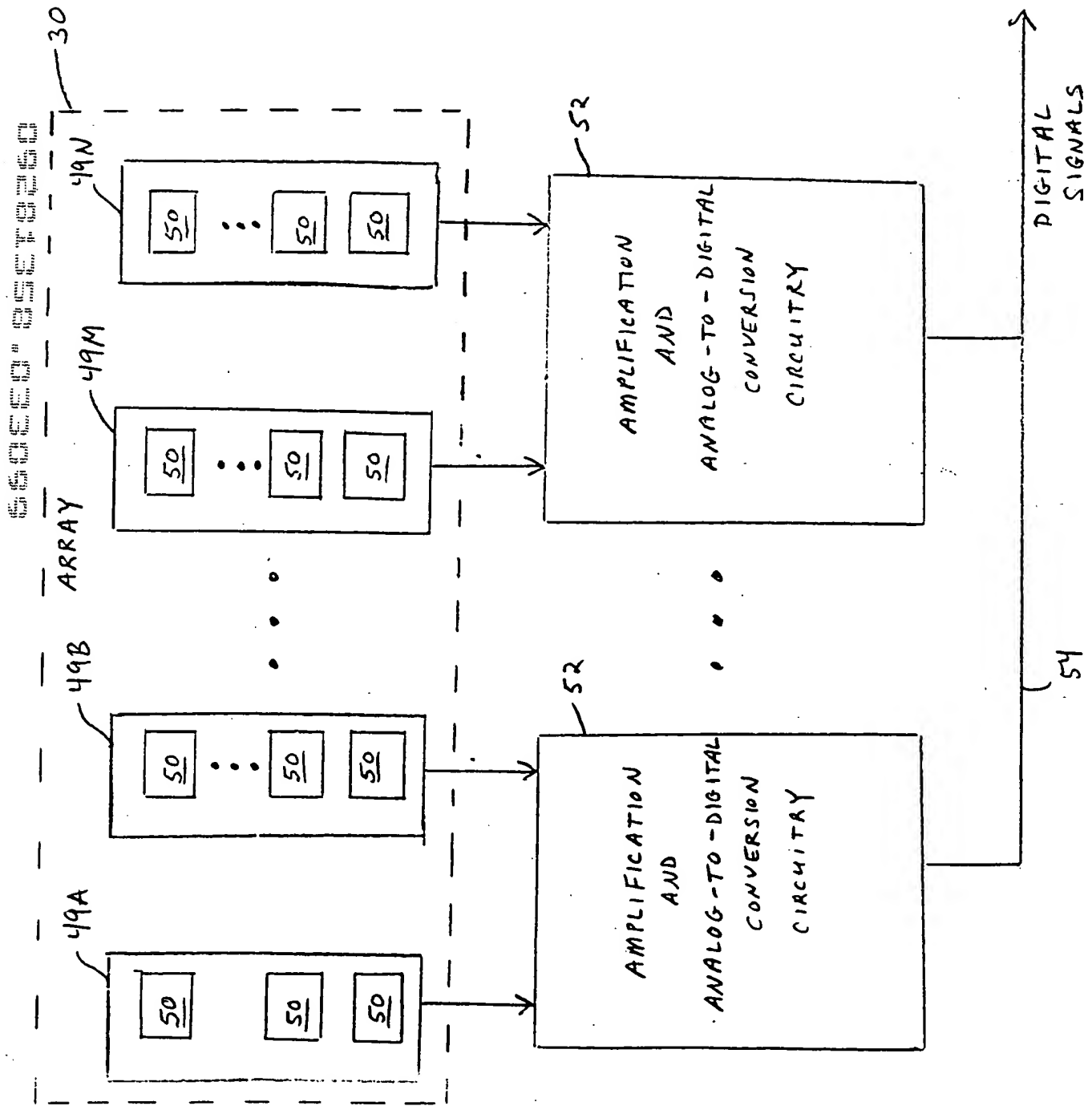


FIG. 2

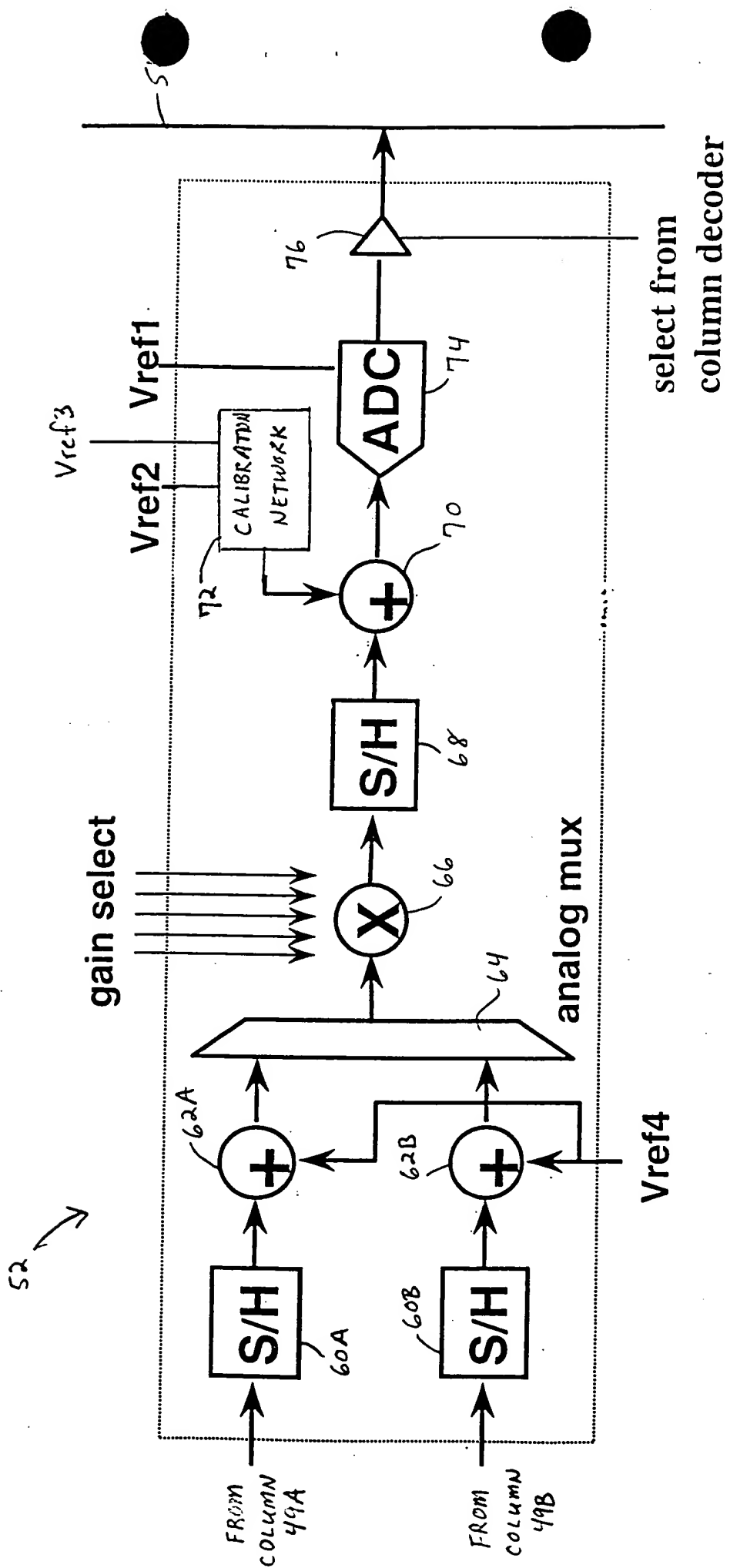
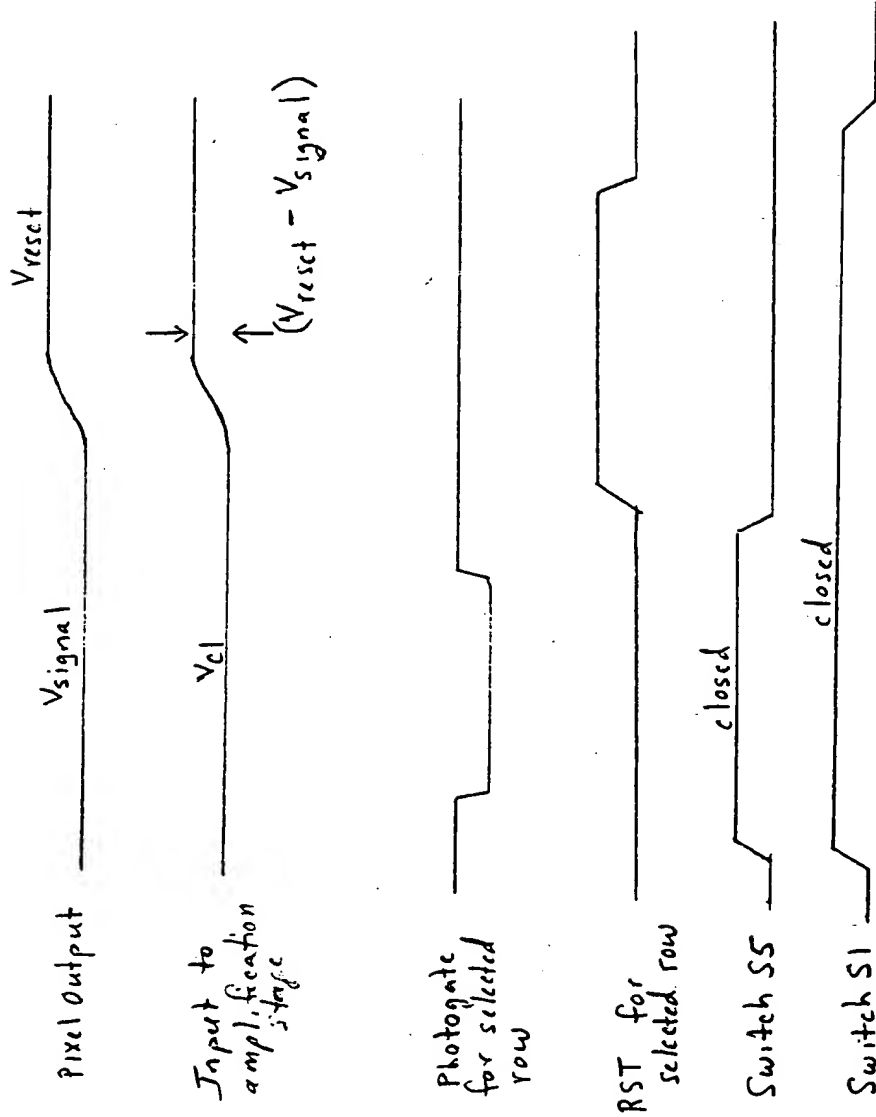


FIG. 3

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SAMPLE AND HOLD TIMING

FIG. 5

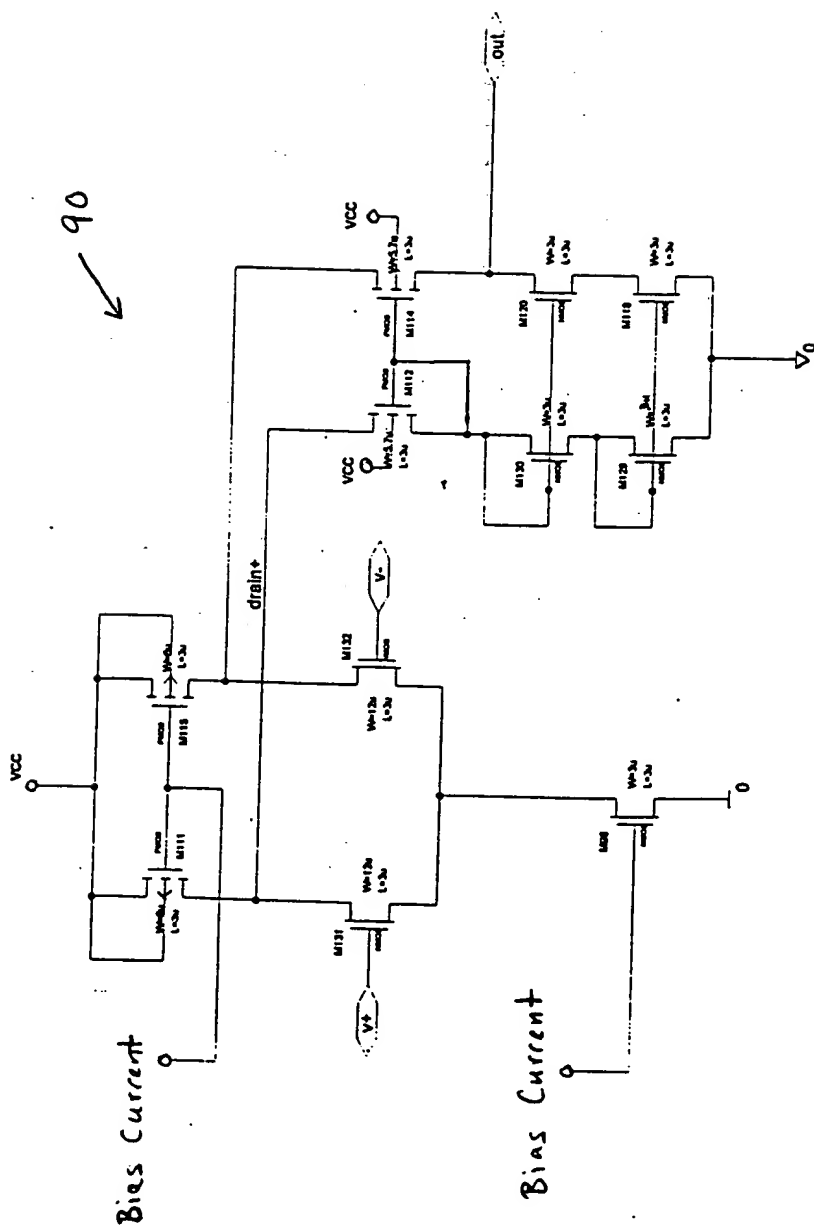
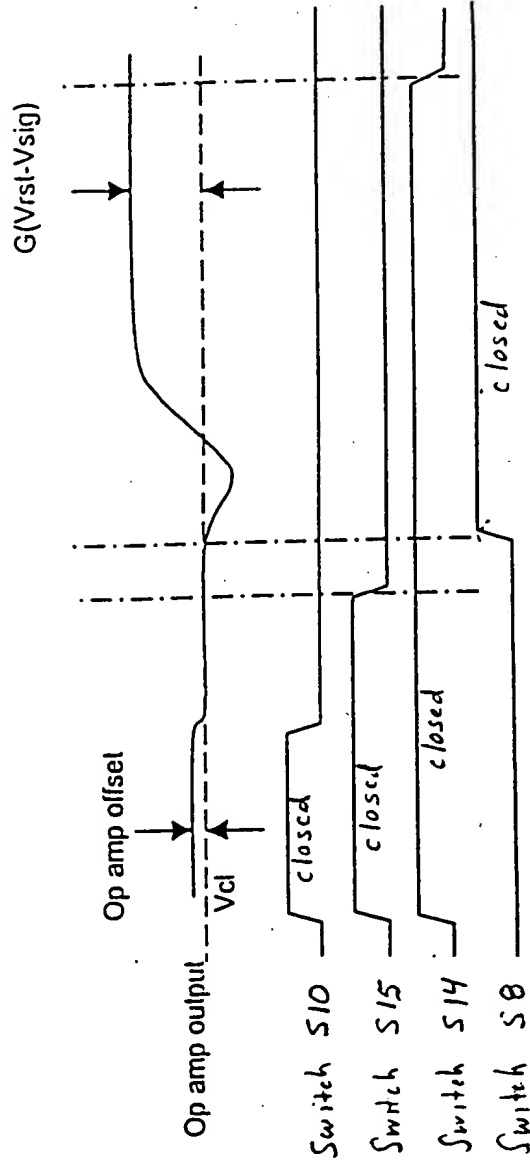


FIG. 6



Amp lification Timing

FIG. 7

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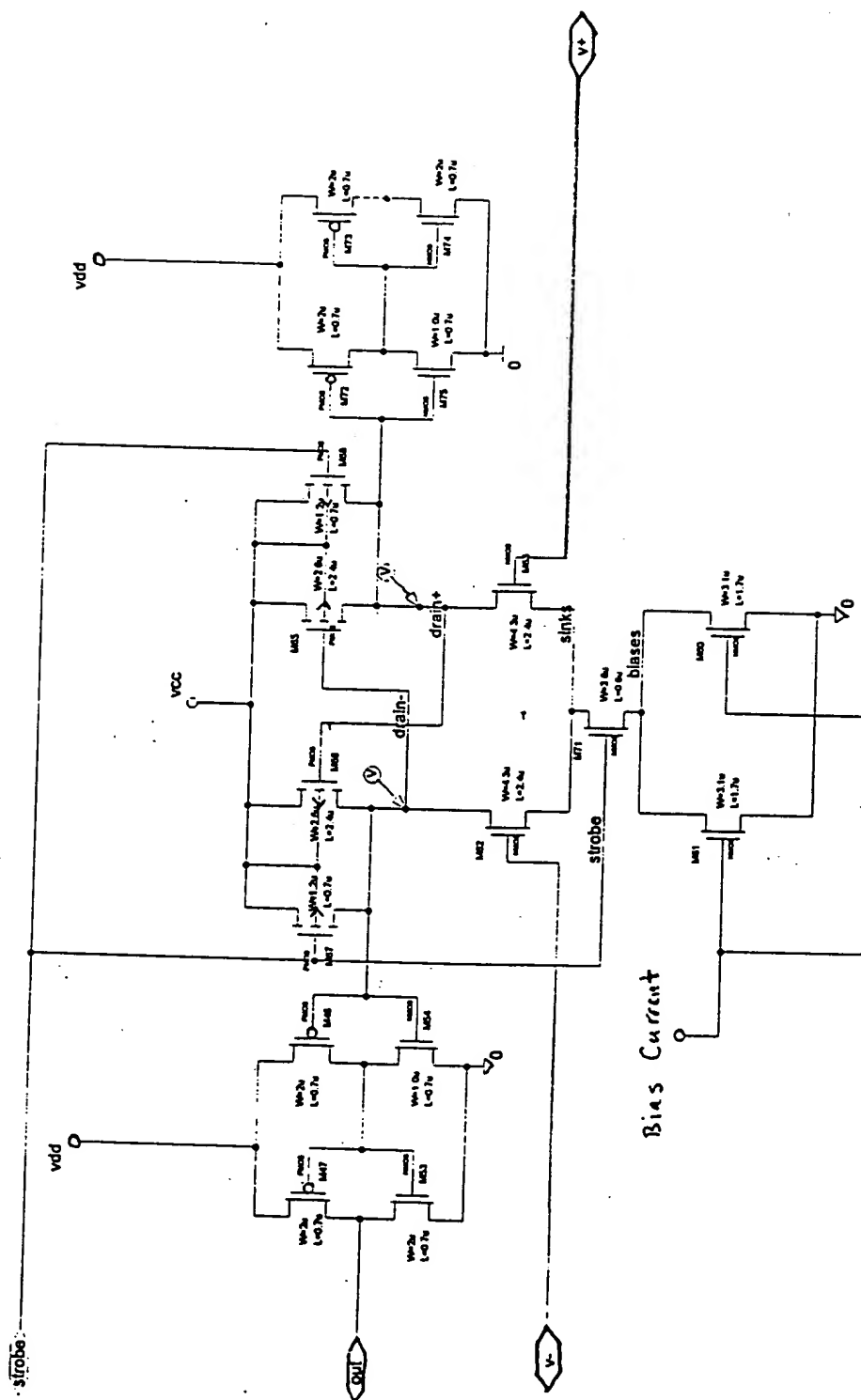


FIG. 8

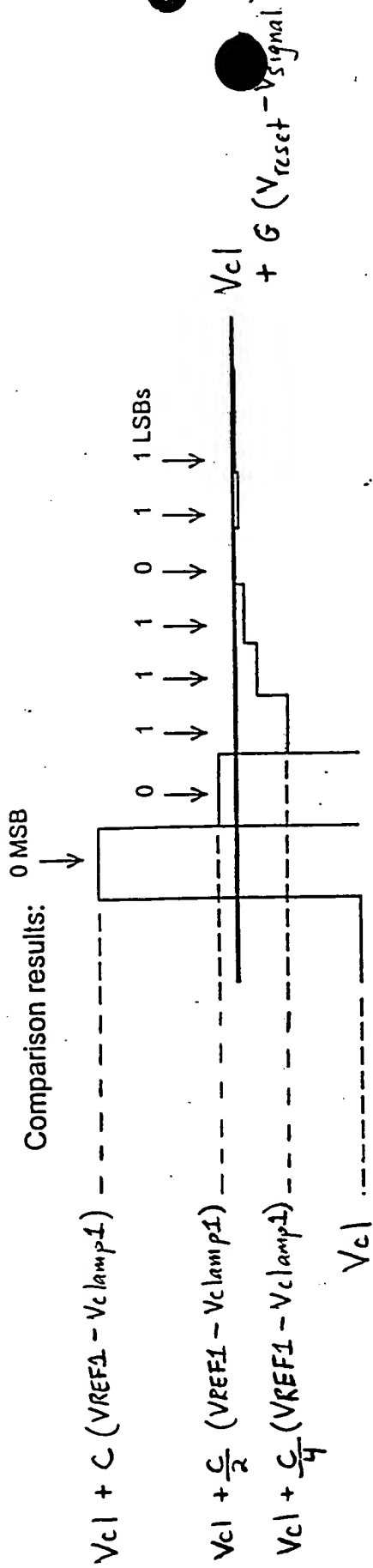


FIG. 9

To negative terminal  
of comparator q2

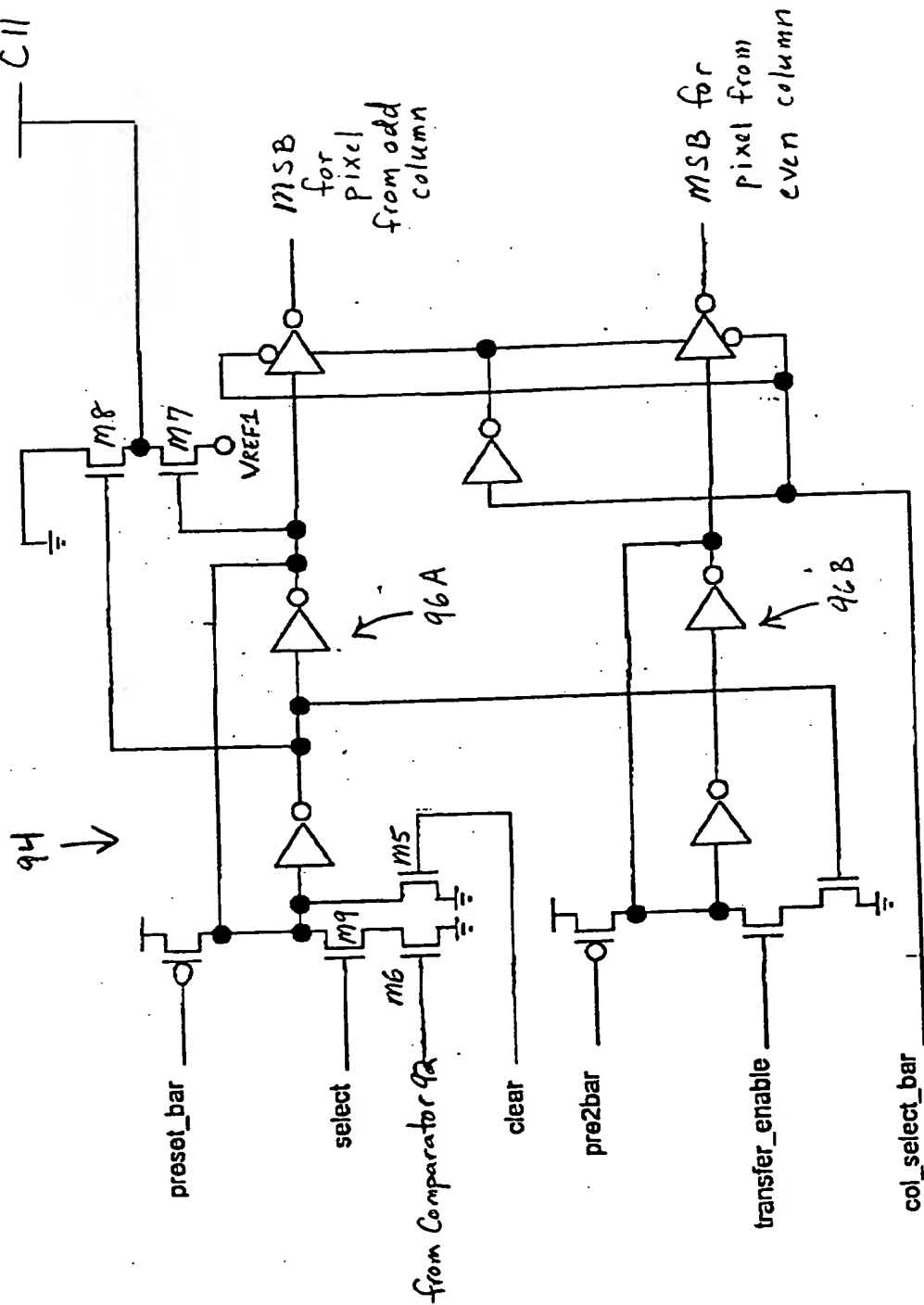


FIG. 10

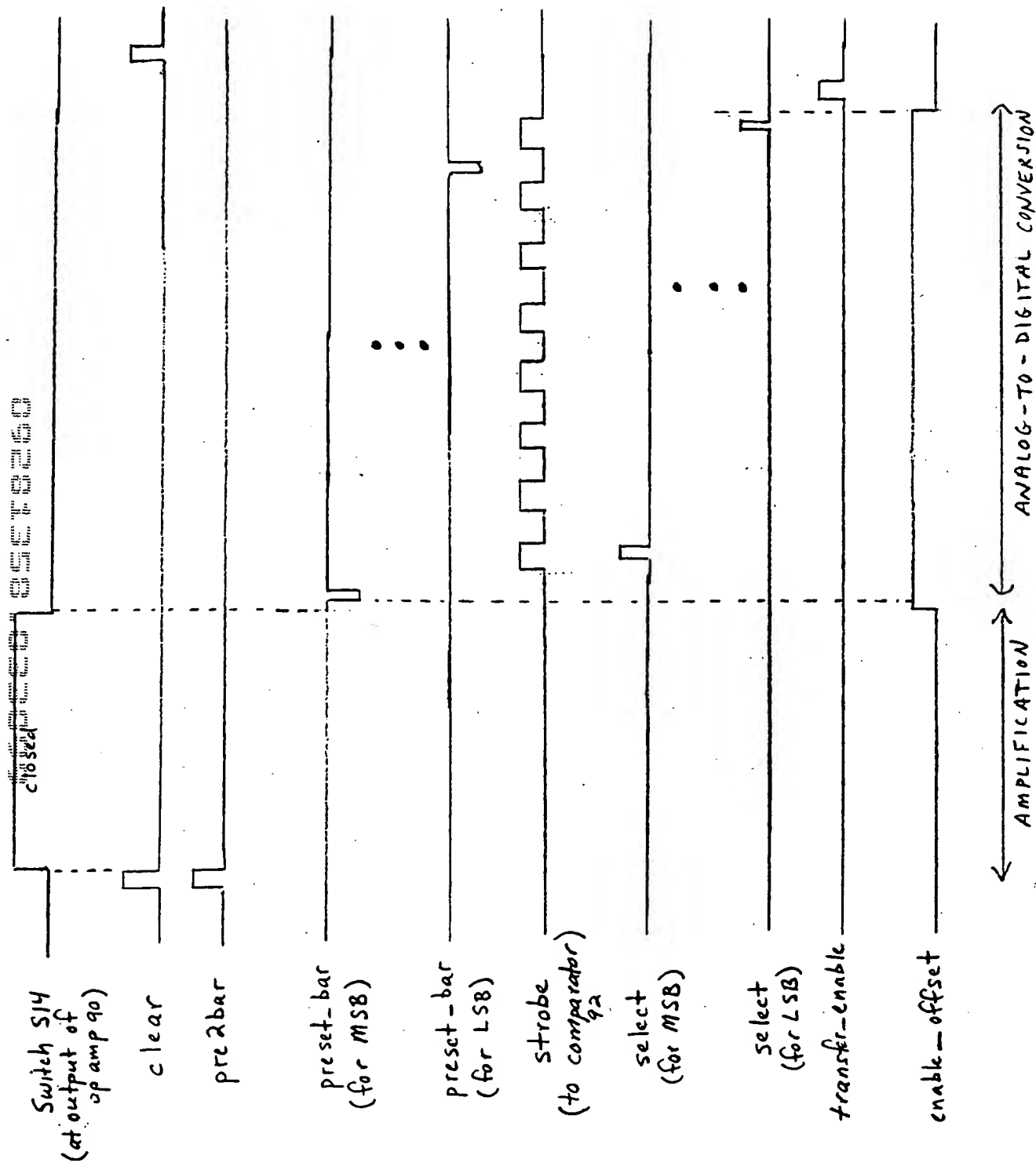


FIG. 11

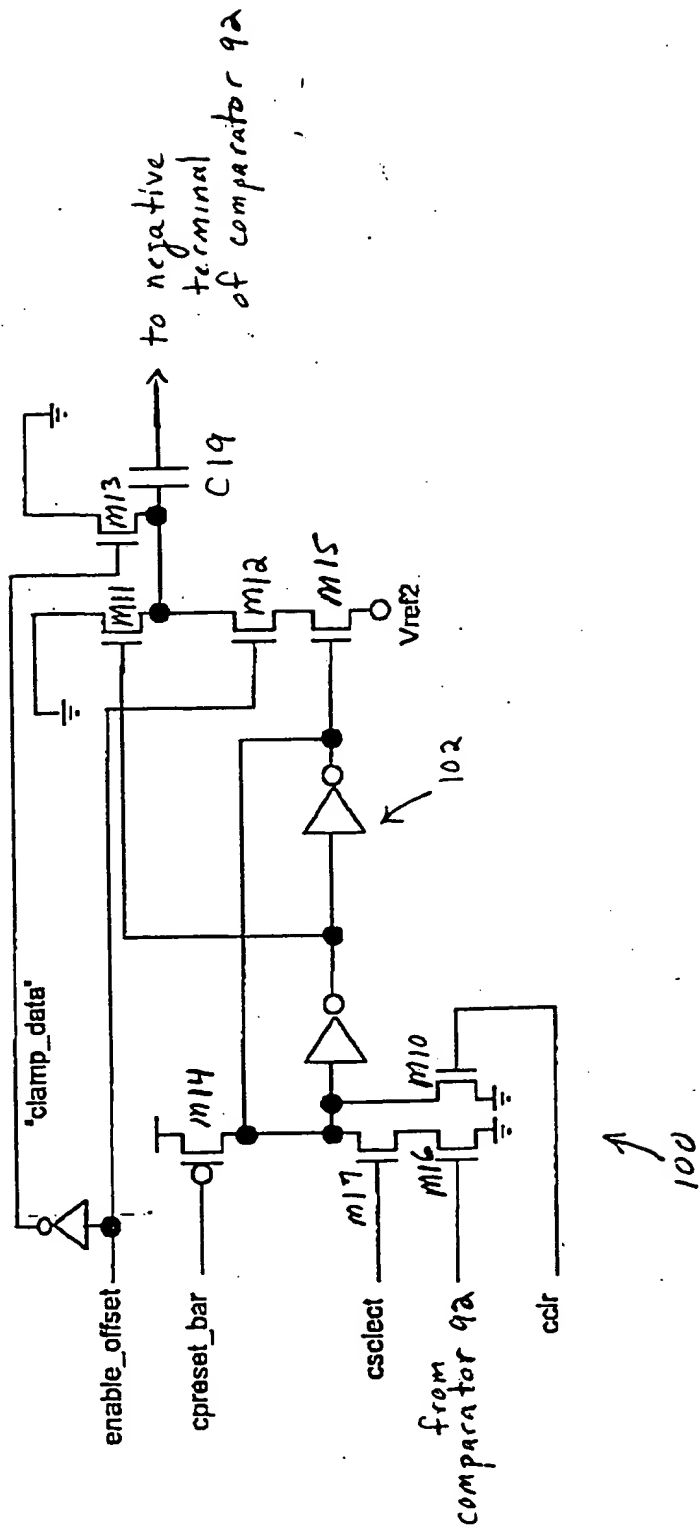
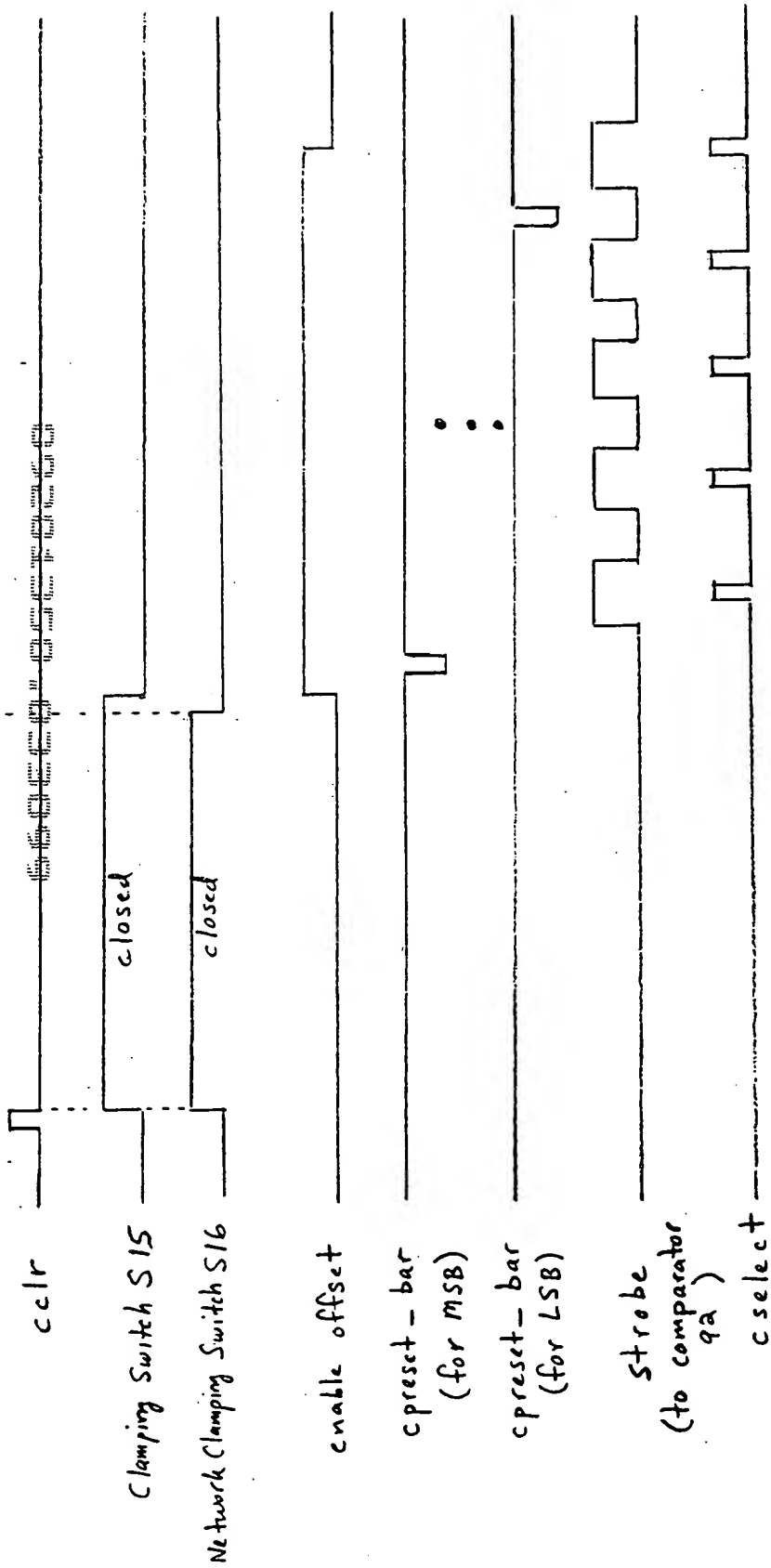


FIG. 12



CALIBRATION TIMING

FIG. 13

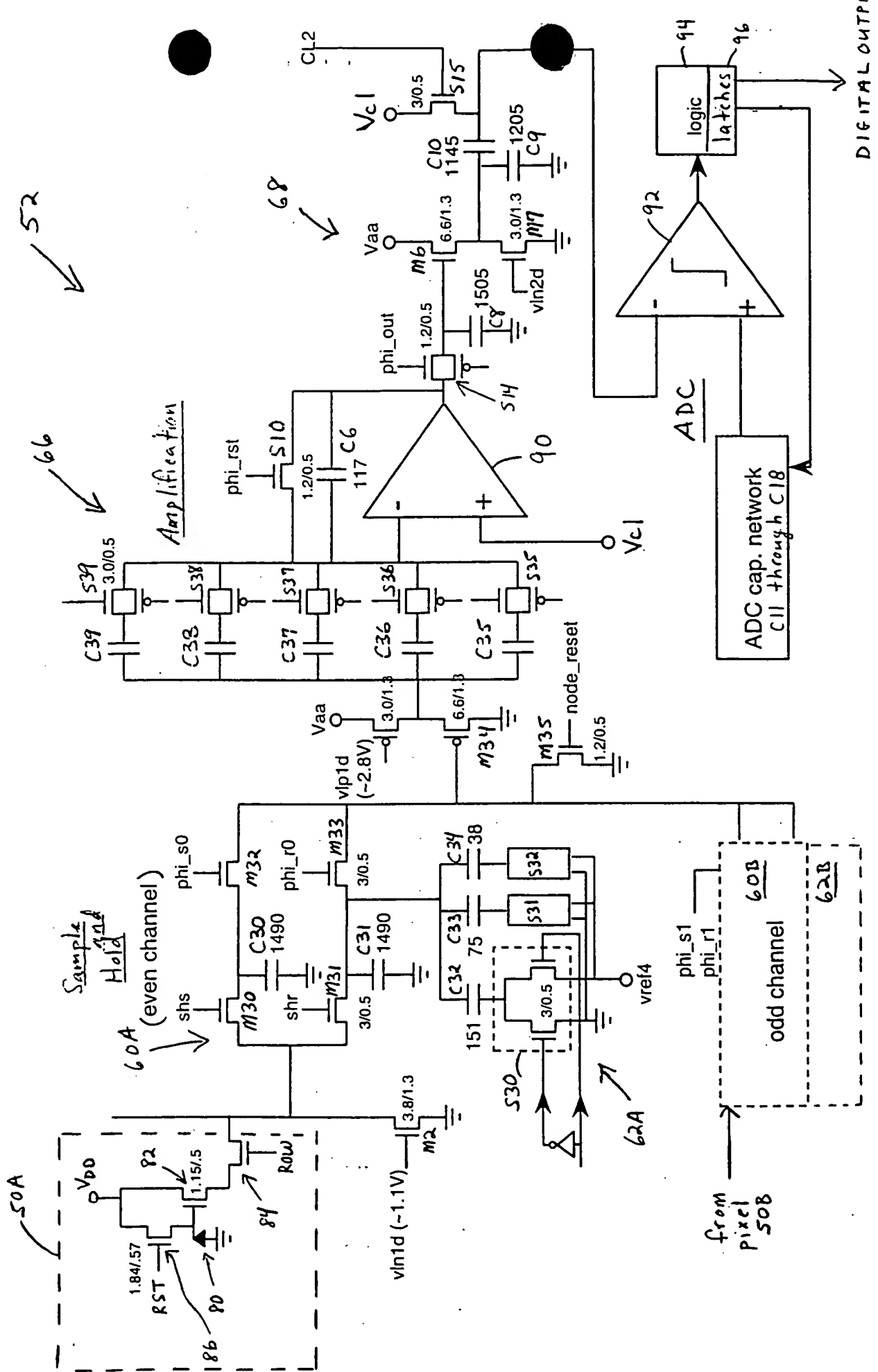


Fig 14

# pixel timing

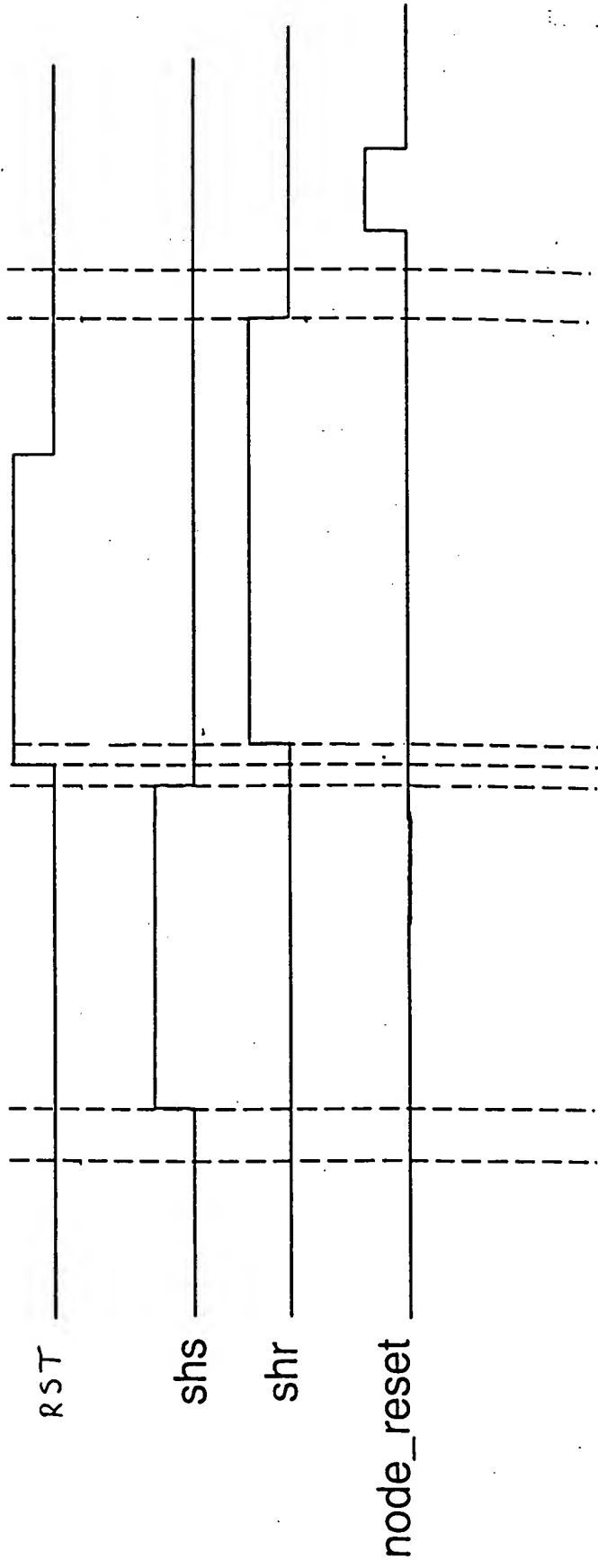


FIG. 15

# gain timing

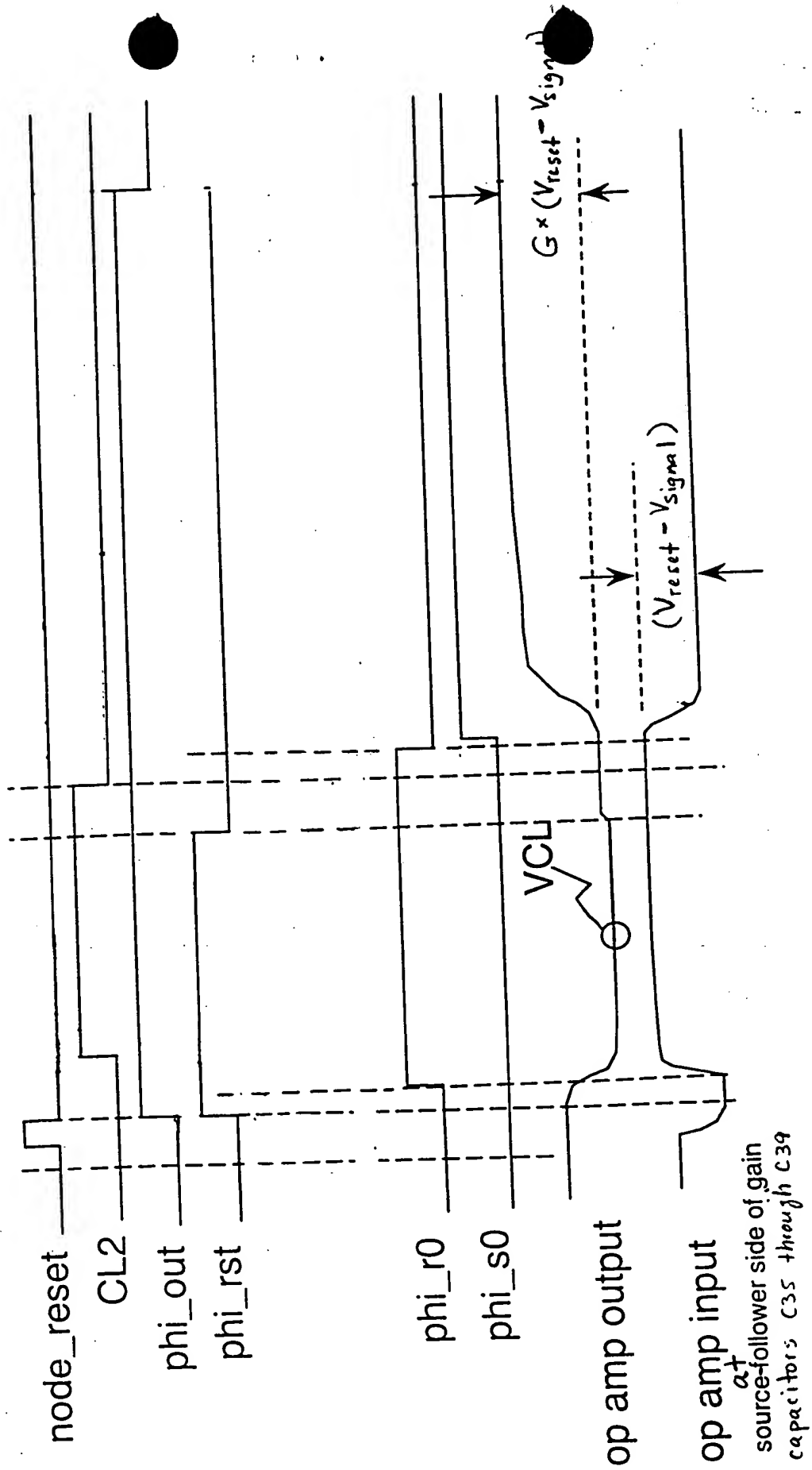


FIG. 16

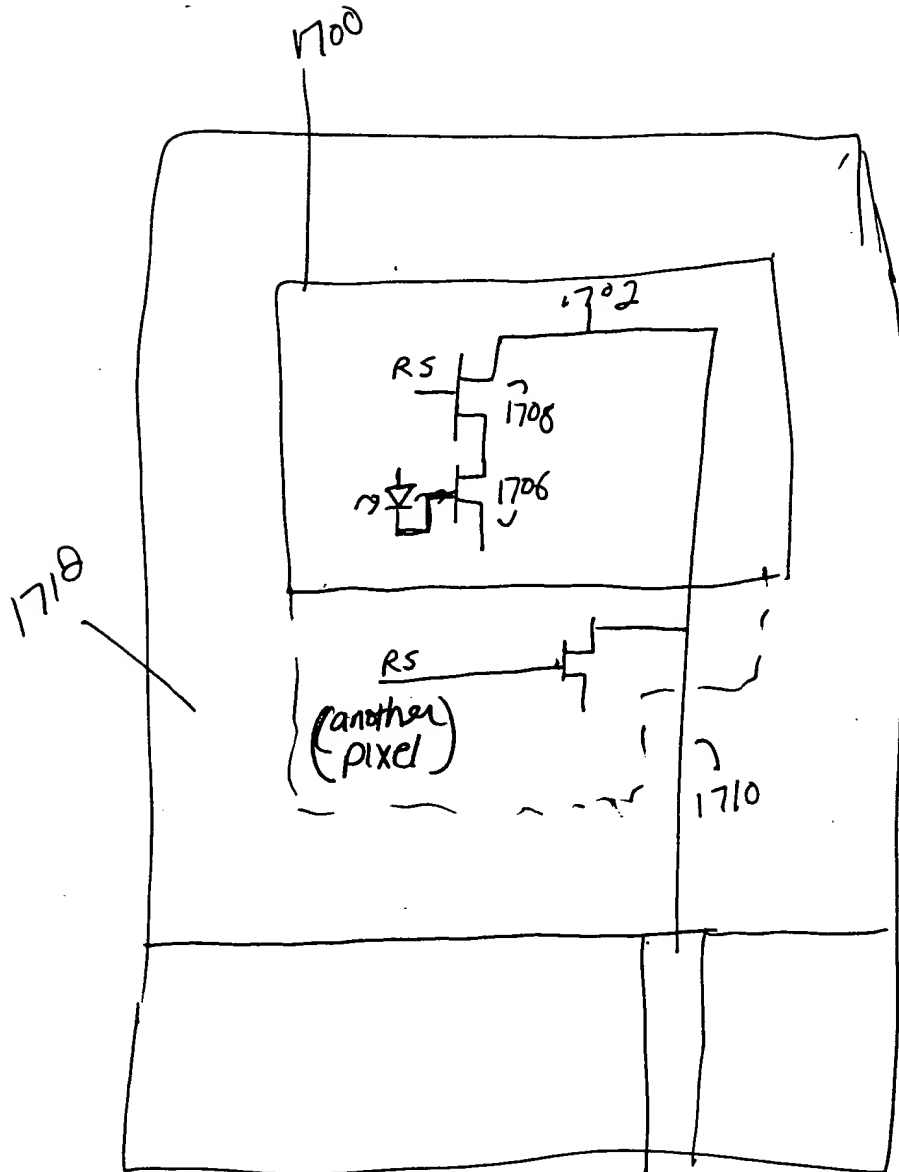


FIG 17

2 Byte Storage ADC  
3/30/98 R. Panicacci